A High-Power 300W Class-AB RF power Amplifier

Seyed Alireza Mohadeskasaei [(1)], and Dragos Dancila [(1,2)]
(1) FREIA, Department of Physics and Astronomy, Uppsala University, Sweden
(2) Microwave Group, Department of Electrical Engineering, Uppsala University, Sweden

Summary

This article presents the simulation and implementation of a power amplifier based on LDMOS semiconductors, operating at 3 GHz and providing a pulsed power of 300W with a signal gain as high as 15dB. The load/source pull techniques are utilized to find out the optimum input and output impedances. In addition, stepped-impedance theory is also used for designing the output and input matching networks. As a result of these capabilities, the amplifier is able to deliver a remarkable 300W with 15 dB signal gain at 3 GHz.

1. Introduction

In recent years, LDMOS (Laterally Diffused Metal-Oxide-Semiconductor) technology has emerged as one of the best option for high power RF amplifiers due to its high efficiency, high linearity, and high output power capabilities [1, 2]. In this paper, we present the simulation and implementation of a 300W RF power amplifier based on LDMOS technology operating at 3 GHz. The amplifier is designed to achieve high gain and output power using load/source pull simulation. The stepped-impedance theory is employed for the design of input and output matching networks. We discuss the design approach and simulation results firstly, and highlight the key features and performance characteristics of the proposed amplifier.

2. Simulation, Fabrication, and Measurement Results

To ensure a high output power and excellent signal gain at 3GHz, load and source pull utilities of Advanced Design Software (ADS) are used to find the optimum input and output impedances, and those are matched with 50 ohm using stepped micro strip transmission lines. The simulation results show that the amplifier is capable of delivering a maximum output power of around 55 dBm (300 W) with a gain of 15 dB at a bias voltage of 32V, as it is shown in Figure 1.

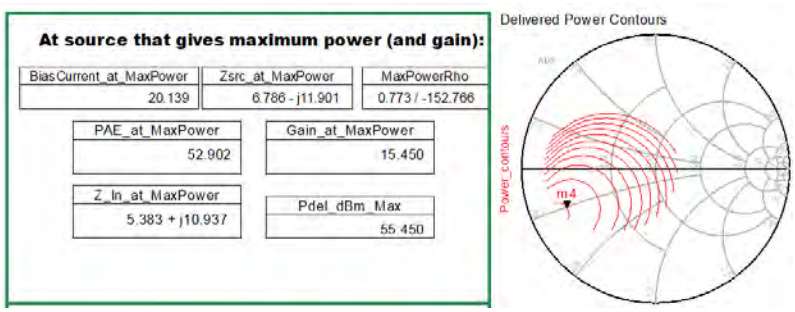
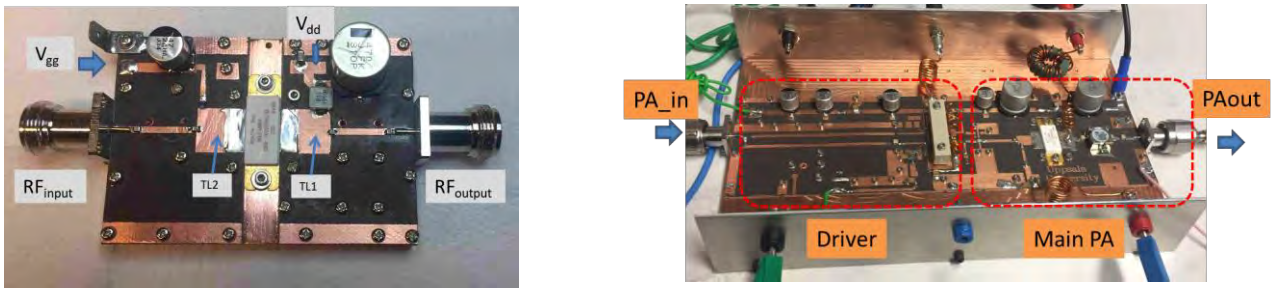


Figure 1: ADS source pull simulation results for the 300 w RF power amplifiers.

The design is implemented on a low loss RF substrate from Taconic, RF-30 with a thickness of 0.030", a dielectric constant of 3, and dissipation factor of 0.002. Figure 2 (a) shows the main amplifier, depicting the initially designed input and output matching networks. To have high gain architecture, a driver transistor with a 25-dB gain is embedded in line up with the main transistor on the PCB. The fabricated RF amplifier prototype including driver and main amplifiers is shown in Figure 2(b).



(a) (b)

Figure 2: Implemented RF power amplifier (a) main amplifier, (b) and RF amplifier including driver and main.

A test bench, as depicted in Figure 3, is used to characterize the power amplifier. It includes an RF signal generator, spectrum analyzer, power meter, and DC power supply. A solid-state high-gain transistor is used in line with the main amplifier, which acts as a power driver, and is embedded on the same PCB. This is necessary since the power provided by the signal generator alone is insufficient. The measurement results for the main amplifier, including and excluding the driver amplifier, are illustrated in Figures 4 and 5. The main amplifier exhibits a 15dB signal gain, delivering 55dBm output power with a 40dBm input signal.

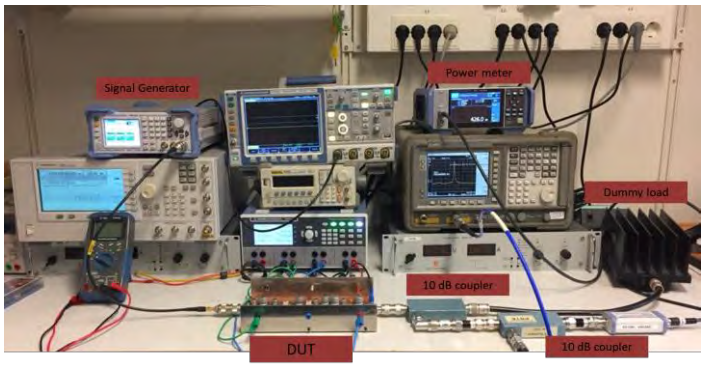


Figure 3: Test bench for characterizing the 300w RF power amplifier.

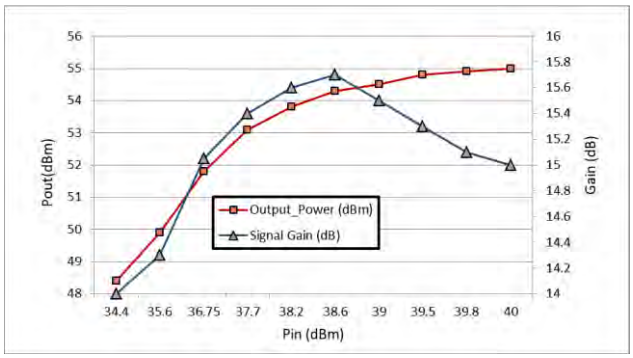


Figure 4: Characterization of main power amplifier excluding the driver.

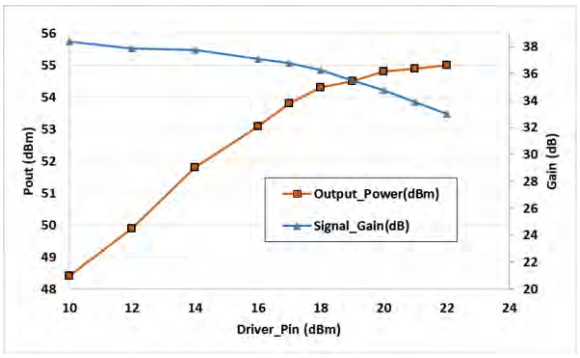


Figure 5: Characterization of overall power amplifier including the driver with 25-dB gain.

3. Acknowledgements

Funding for this project was provided by the Swedish Research Council for the project entitled "Development of an RF-system for the AWAKE-Run2" under project agreement No. 2020-06161.

References

[1]. Tong, Renbin, et al. "Kilowatt Power Amplifier With Improved Power Back-Off Efficiency for Cyclotron Application." IEEE Transactions on Microwave Theory and Techniques 70.2 (2021): 1401-1409.

[2]. S. Cimino et al., "Optimized LDMOS Offering for Power Management and RF Applications," 2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2022, pp. P57-1-P57-5, doi: 10.1109/IRPS48227.2022.9764528.